Yield Modeling and Patterns Prediction using Data Mining: a Preventive Approach

Vincent Barec, François Bergeret, Alexandre Couvrat

We will introduce first the context and the two companies that have developed the methods, then we will present Yield Model, principle and one application. We will then present Pattern Prediction, the methods used and two applications. Conclusion and perspectives will conclude this paper.

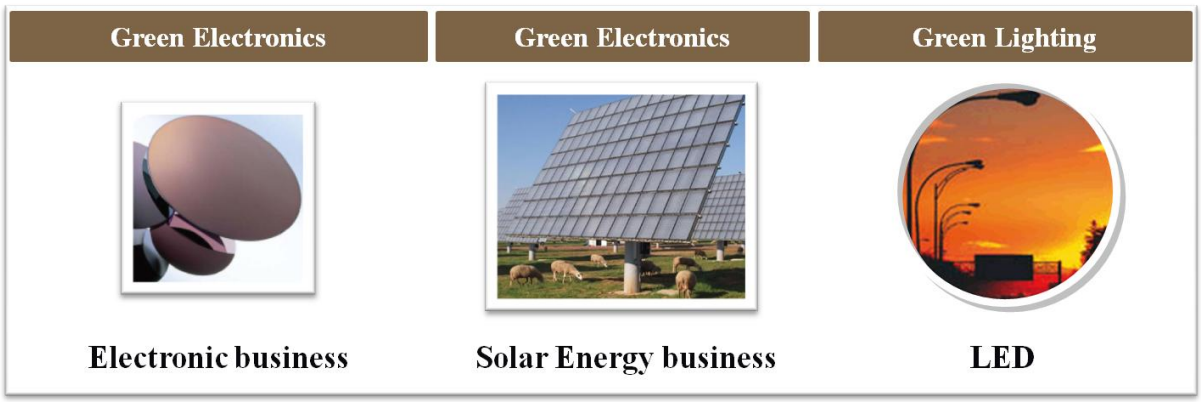
Introduction

Soitec is the world leader in generating and manufacturing revolutionary semiconductor materials for electronic and energy industries. As an industrial company, we have built our reputation developing and manufacturing our flagship material, SOI (Silicon-on-Insulator).

Jean-Michel Lamure and André-Jacques Auberton-Hervé founded Soitec in 1992 to develop and commercialize the revolutionary Smart Cut™ "atomic scalpel" technology. Since then, the company has continued to innovate and grow. Today we are leading technological advances that will shape the performance of tomorrow's products on markets like computing, telecommunications, automotive electronics, and lighting. Our Concentrix™ technology has also enabled us to become a global leader in the manufacture of systems used by the concentrator photovoltaic (CPV) solar energy industry.

Soitec is a truly international company, with:

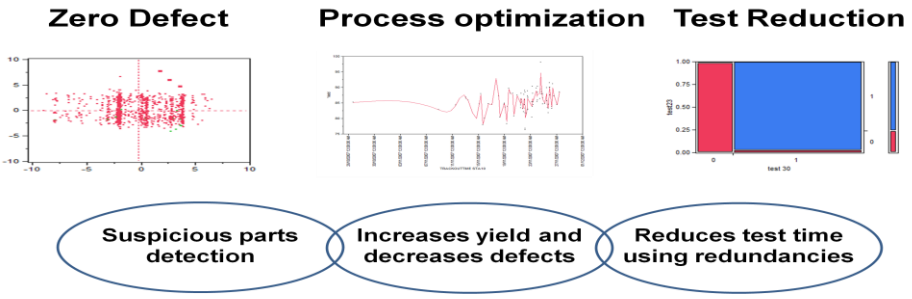
- R&D and industrial manufacturing activities in France, Germany, Singapore, and the United States
- A customer base that includes global microelectronics and energy leaders located on five continents (more than 90% of our revenues come from export sales)
- Employees representing 25 nationalities working in more than 10 countries



SOITEC activities

Ippon Innovation is a consulting and software company based in Toulouse, France. Ippon proposes consulting services for statistics, SPC, process and yield optimization... Ippon also

develops advanced software, JMP-based, to improve quality and reliability, to reduce test time and to improve processes and yield. This kind of applications will be presented in this paper.



Ippon Innovation software activities

A long term collaboration between SOITEC and Ippon has been started 4 years ago, with several achievements including:

- Yield Guard, a statistical tool used weekly to detect any process tool responsible for yield losses.

- Drift Detector, an innovative program able to detect a process stage responsible for a drift.

- Yield Toolkit, a suite of JMP-based tool to secure the qualification, to screen continuous parameters correlated to a response ... The set of tool is presented in the next figure.

The tools presented in this paper a new development that takes into account the need from SOITEC for a more preventive approach.

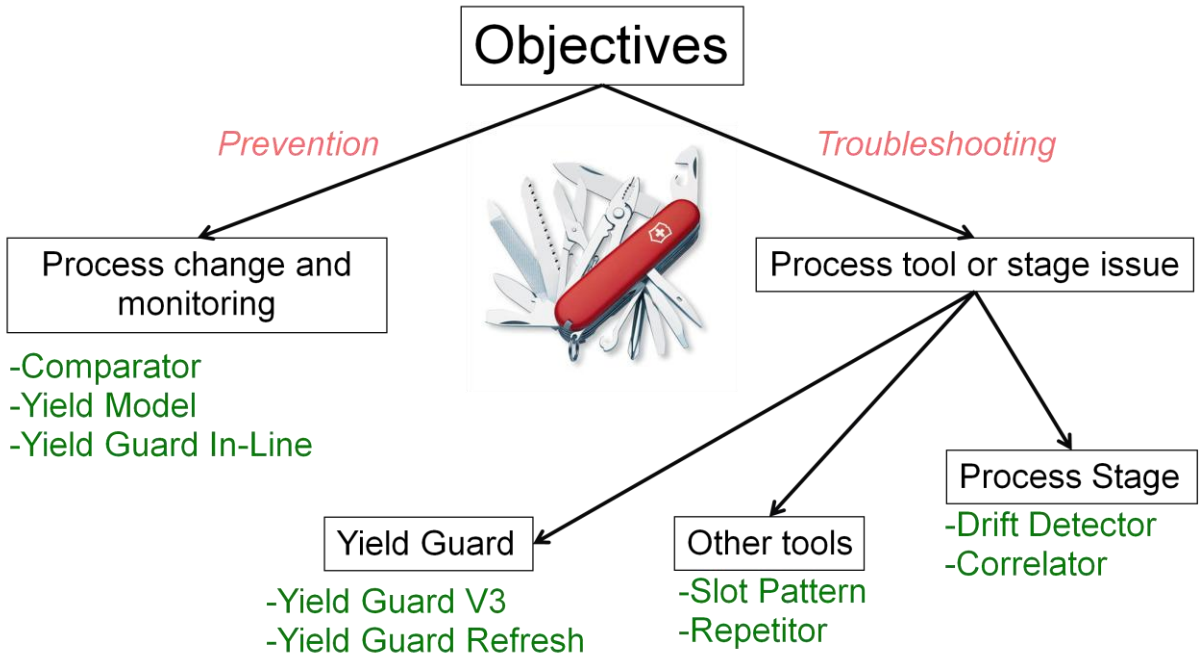


Figure 1: the set of existing tools at SOITEC, Pattern Prediction will be included soon

Yield Model

Systematic data analysis to improve yield has been used for years [1] with very good results. In a previous presentation [2] we have developed Yield Guard, used to detect any process tool responsible for yield losses. Yield Guard is automatically performing a set of statistical tests adapted to the nature of the response distribution (normal, non-normal, binary), and summarizes the results with graphical outputs to help the engineers to find the root cause of the issue. Next graph illustrates Yield Guard results.

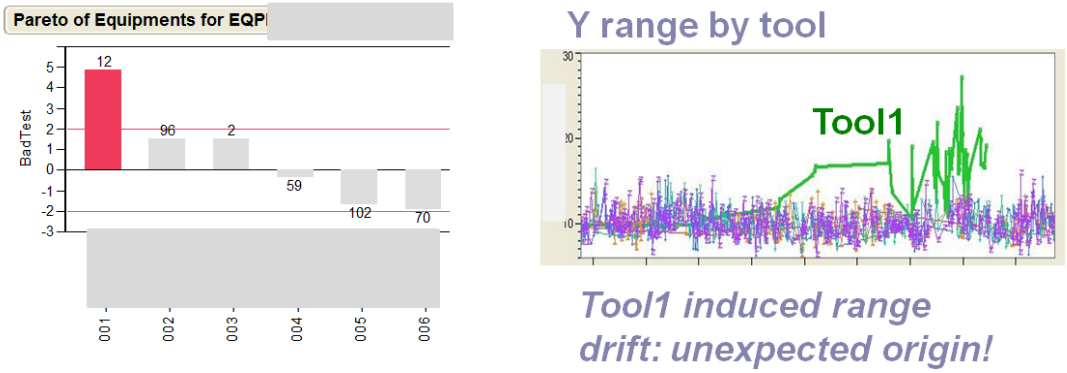


Figure 2: Process Tool 001 in red is statistically the bad tool. Time line on the right is a time visualization of the effect (Tool 001 in green, X-axis is the process date, Y the response).

Yield Guard is very useful to explain yield losses, but there was a need to predict future variations. In that context, we have developed Yield Model that is working this way:

- Yield Guard is run to detect significant effects on the yield

- These parameters are used to create a global model (ANOVA)

- Users are then able to add or remove some effects based on engineering expertise.

- For complex effects, users can merge some them at will and create some “big classes” like good and bad tool at stage 1, good and bad tool at stage 2…

- Users can also enter production parameters: the number of lots that will be process by different tools next month for example

- The final model is run, using the effects detected by Yield Guard, and the production information.

- Yield Model will provide users with prediction for next month, and new simulations are also possible based on production and yield scenario: the best trade-off can be found.

In the below example, a Yield Guard analysis was performed and highlighted statistical effects from both supplier and equipment_Stg4 on the percentage of wafers without any

defect. As performance get stable over weeks for any supplier and any equipment_Stg4, user was able to merge suppliers with same performance and equipments_Stg4 with same performance among best and worst groups. Graphical output 3 highlights the production mix of the different class combinations over weeks; explaining the variation of the global variable as show in in figure 3.

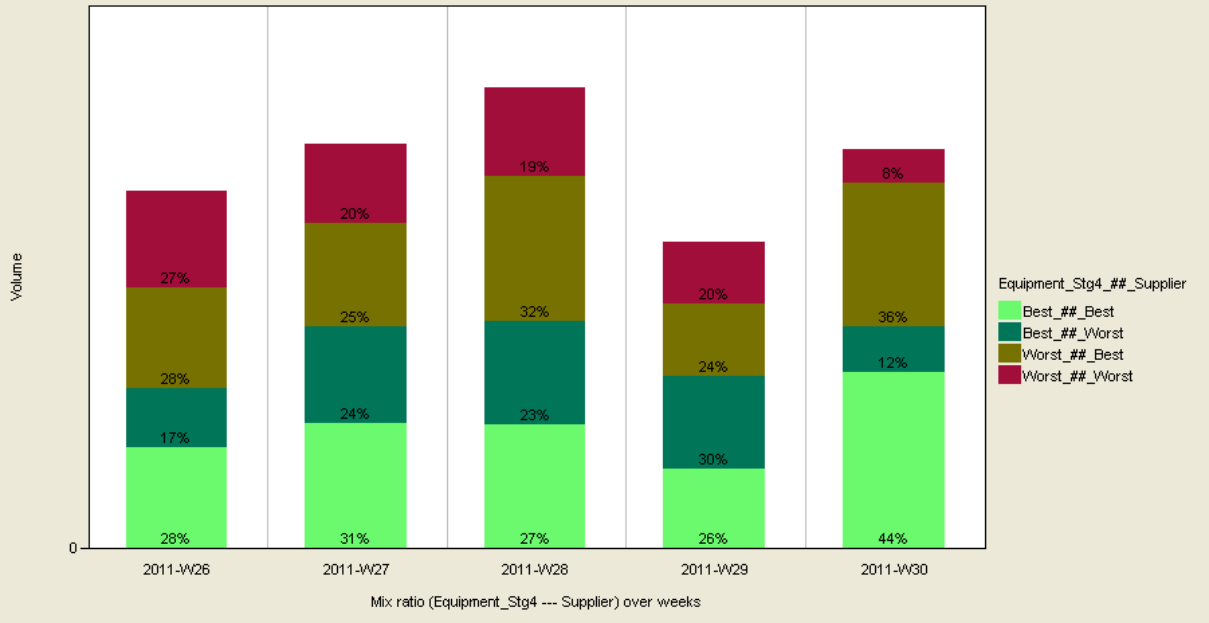


Figure 3: Yield Model Output

Accurate yield predictions can be obtained, with the impact of a bad mix as shown in figure 4.

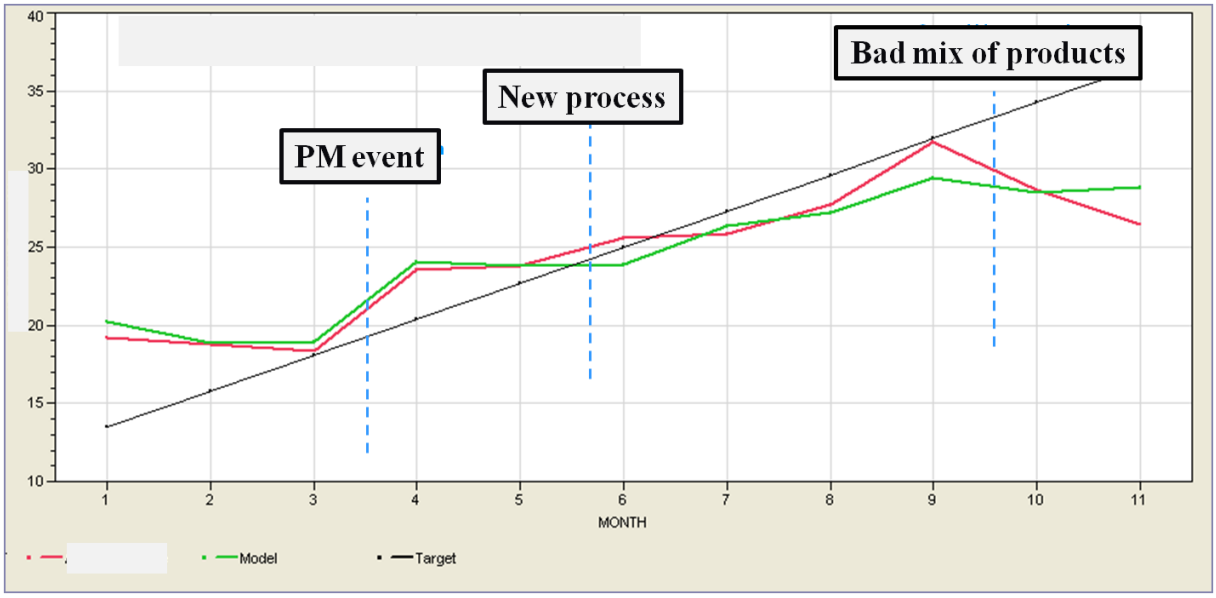


Figure 4: Predictions

Pattern Prediction

Wafer patterns (also call wafer maps in this paper) are very important in semiconductor manufacturing, because they characterize the geographic effect of different process stages on the finished part: a wafer.

Process issues that can appear are divided in two different categories:

- Parametric issue, for example when the thickness is not homogeneous on the wafer

- Defectivity issue, for example when a given pattern of particles occur

In the next figure, a parametric wafer map is provided, it is a thickness map.

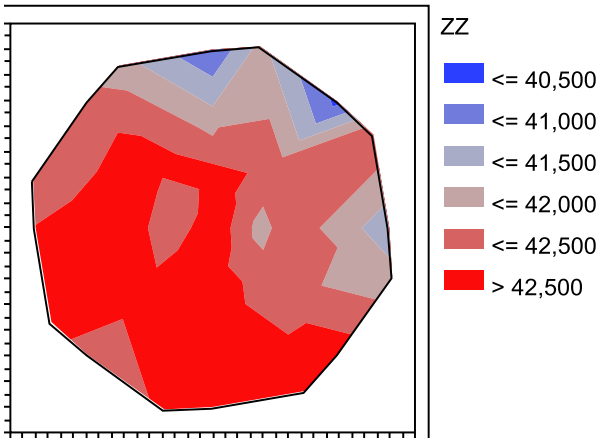


Figure 5: a wafer map: blue zones are low thickness areas, the pattern here is a blue zone on the upper side of the wafer

Pattern Prediction on thickness maps

Pattern Prediction is working like this on parametric wafer maps:

- A training set is used: the user provides the software with known patterns, i-e patterns that have been classified by the human brain

    - X factors is the thickness measured on several points (more than 30) on the surface of the wafer

    - Y response is a binary variable: presence or not of a given pattern (like the one is the previous graph)

- A neural network is then used to learn from this sample. More details on neural nets can be found on a large number of papers, for example [3].

- A validation set is then used to check the prediction accuracy. In this application, the global error rate should be lower than 10%, ideally lower than 5%.

A two-layer neural net is presented in the next application, the sample size for the training set is not large enough but the global error rate is lower than 10%

Model NTanH(3)NTanH2(3)

Training

MAP	Measures
Generalized RSquare	0,9693812
Entropy RSquare	0,9576553
RMSE	0,0319902
Mean Abs Dev	0,0130221
Misclassification Rate	0
-LogLikelihood	0,6926922
Sum Freq	51

Confusion Matrix

Actual MAP	0	Predicted 1
0	46	0
1	0	5

Validation

MAP	Measures
Generalized RSquare	0,8897411
Entropy RSquare	0,8164754
RMSE	0,1803953
Mean Abs Dev	0,0762176
Misclassification Rate	0,0833333
-LogLikelihood	2,4768554
Sum Freq	24

Confusion Matrix

Actual MAP	0	Predicted 1
0	17	1
1	1	5

Figure 6: neural net results: one false negative and one false negative on the validation set

Pattern prediction on defect maps

The problem is the same: detecting a pattern. It is very important to develop and automatic pattern detection for two reasons:

1- The person is charge of pattern detection classifies around 1000 wafers per week, spending half a day per week to a tedious task.

2- The classification is human-dependant: trials with other persons lead to other classifications!

The method used here will be different compared to the parametric wafer maps because the X variables are the defects on the wafer, and the number of defects is not fixed, it is highly variable from one wafer to another. For that reason we are developing a new method still based on neural nets, described below, but other alternatives are investigated, based on spatial correlograms [4].

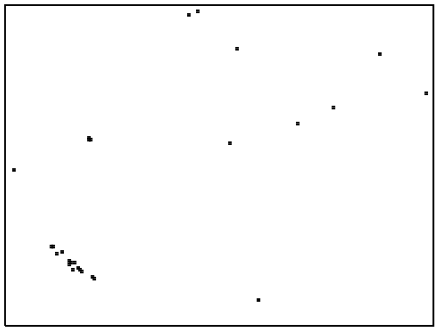


Figure 7: an "ear ring" pattern: cluster of particles on the lower left part of the map

Method for the defect map prediction based on defect statistics and neural net

- For each wafer, statistics are calculated: number of defects, average location... and geographic statistics not detailed here for confidentially reasons

- A training set is used: the user provides the software with known patterns, i-e patterns that have been classified by the human brain

    - X factors statistics calculated per wafer

    - Y response is a binary variable: presence or not of a given pattern (like the one is the previous graph)

- A neural network is then used to learn from this sample.

- A validation set is then used to check the prediction accuracy. In this application, the global error rate should be lower than 5%.

- Boosting methods available in JMP Pro can be useful to improve the predictions: boosting builds a set of model and each model is improved from the previous one because miss-classified observations are more weighted.

A two-layer neural net with boosting is presented in the next application, the sample size for the training set is not large enough and the global error rate is close to 10%

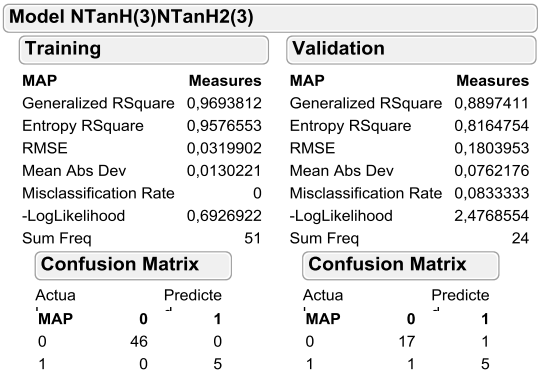


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Figure 8: neural net with boosting applied to defect maps: 2 wafers are miss-classified

Conclusion and perspectives

Yield Model is working in production mode at SOITEC, future developments will take into account continuous parameters and interactions in the model to improve even more the prediction accuracy.

Pattern Prediction are already working with good results in terms of error rate.

Parametric maps can be improved by developing an automatic classification of the wafer maps without learning. Methods exists in other industries and we are working to adapt them to semiconductor.

For defect maps, neural net approach is working well and will be released to production. the approach based on spatial correlograms seems very promising and we are going to test it on production data.

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Authors

Vincent Barec works as a defectivity engineer for Soitec, a high tech semiconductor company supplier of engineered substrates, since 2005. Defect reduction and yield improvement are his main missions. He is graduated from the Grenoble Institute of Technology (France, 2005).

François Bergeret holds a PhD in statistics from Toulouse university and he is Motorola six sigma black belt. He worked for 13 years in Motorola and Freescale, he is now consultant for high tech companies, including semiconductor. He founded Ippon Innovation in 2007, developing solutions for yield, test time reduction and zero defect.

Alexandre Couvrat graduated from the Engineering School of chemistry and Physics from Bordeaux, France in 2000. He worked for Philips Semiconductors during 6 years – now titled NXP Semiconductors- as a defectivity engineer focusing on defect reduction and metrology tool ownership. In 2007, he joined Soitec, a high tech semiconductor company supplier of engineered substrates, as a senior yield engineer. His main mission is yield enhancement though close follow-up of product parameters.