The Turning of JMP® Software into a Semiconductor Analysis Software Product:

The Implementation and Rollout of JMP® Software within Freescale Semiconductor Inc.

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Author Biography

Jim Nelson's career started as a resident research analyst for North Dakota State University. From there he went to work for SAS Institute in the education area, ending up as the Director of the Austin SAS branch office. He joined Motorola in 1991 and then Freescale Semiconductor when it was split into a separate company. Jim has been using the SAS product since 1973, and JMP® software since the 1990s.

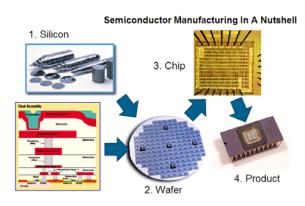
Abstract

The semiconductor manufacturing environment is a very specialized area of manufacturing. Fabrication of a computer integrated circuit is a very complex process. Chemical, photographic, mechanical, electrical and spatial factors all have to intersect in a highly choreographed process to produce a working computer chip. The process of optimizing the yields or investigating unexpected yield losses requires both specialized data visualization tools and sophisticated statistical analysis to quickly find the root causes. "Out of the Box" JMP® software is not a "Semiconductor Analysis Software Product". While a skilled engineer can manipulate their data and manipulate the various JMP software platforms to approximate the required visualizations and analyses, today's market place does not permit such a time consuming process. Engineers need analysis tools that quickly provide the precise visualizations and analyses they need with the fewest number of mouse clicks. This paper details the processes, additions and modifications made to JMP software to turn it into a "Semiconductor Software Analysis Product".

Introduction

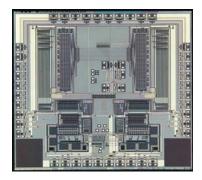
Integrated circuit manufacturing is a complex process, taking hundreds of steps from a raw silicon wafer to a packaged, integrated circuit, most commonly referred to as a computer chip. A brief description of this process will help with the understanding of why specific visualizations and analyses had to be added to JMP® software to make is a viable tool for the semiconductor industry.

Silicon wafers are the starting material in the manufacturing of integrated circuits. They are round slices of silicon and come in various sizes. 150mm, 200mm and 300mm wafers are used in the manufacturing of ICs for Freescale.



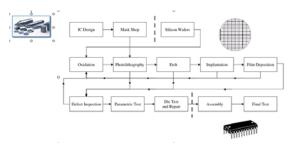
Within Freescale, 25 wafers are processed together, which makes up what is referred to as a "Lot". Each wafer within the lot will have hundreds to tens of thousands of individual ICs fabricated on it. Each of these individual replicates is referred to as a die.

The basic process is very similar to the making of a circuit board, like the motherboard of a computer, except on a very, very, very small scale. The line sizes are not measured in millimeters, like on a motherboard, but in nanometers. 1mm equals 1 million nanometers.

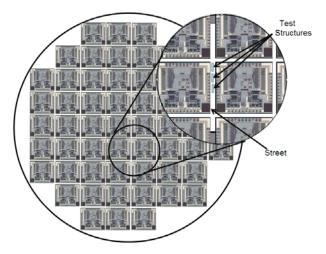


Various steps are used to photographically lay down circuits on the silicon and to selectively remove or add material to make the circuit. Then, an insulator layer is placed on top of the circuit for either protection or insulation from additional circuit layers that will be laid on top of each other to complete the full circuit required for the individual IC being produced.

Thousands of measurements are recorded on each wafer as it moves through the fabrication and assembly process.

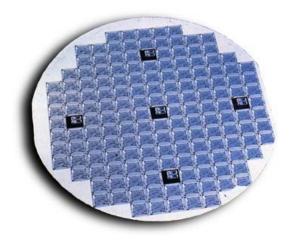


While the individual wafers are being processed, measurements are made on the physical aspects of the process. Typically, each process step has associated measurements taken to determine the accuracy of that step in the process. Additionally, during various stages in the process, test structures that are built in the spaces between the die (streets) will be measured to determine if the manufacturing process is within the specification limits for the product being fabricated.



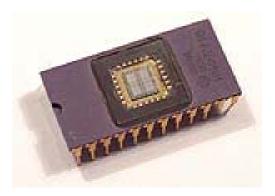
Within Freescale, this is referred to as Class Probe. Other semiconductor companies may refer to this as WAT (Wafer Acceptance Testing), or PCM (Process Control Measurements).

After the fabrication processes are completed, a final Class Probe is performed and then the lot is moved to the Unit Probe step, or what is often referred to as Sort. In this step, complete electrical testing of each die is done to determine if it works (yields) and₂ with some products, if the die works fast enough. A resulting bin is assigned to each die.



All non yielding die are either electrically marked (inked) or physically inked indicating, to the next steps, exactly which of the die from each wafer are to continue on to the assembly and final testing as a completed part.

Assembly and final testing of each die brings with it another whole category of measurements on the parts. (Once a wafer is sawed into individual die and assembled into its packaging, each die is more commonly referred to as a part.)



Within the assembly process there are additional tool measurements, such as the accuracy of the joints in the wire bonding process that solders the die to the electrical pins of the IC package or the temperature of the furnace that is used to mold the top and bottom of the final package together.

During final testing of the assembled product, the part typically has electrical tests performed on it in cold, room temperature and hot environments.

Finally, the product is ready for burn in testing. This testing involves prolonged usage of the part with a variety of typical patterns of usage being run on the product to test for failing parts.

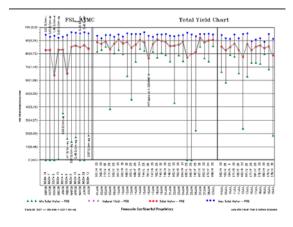
Product that has made it through all of the process and testing steps successfully are then boxed and shipped to the customers.

JMP Software at Freescale

JMP software has been at

Freescale/Motorola since the early 90s as an engineering tool. Its usage was not globally supported and the knowledge and use of the product varied from organization to organization. Concentrated mainly in the US fabrication facilities, it was used for yield analysis and when DOE was introduced into JMP software, it became the primary tool used for experimental analysis. Formal support of JMP software within Freescale started around the timeframe of the release 7 of JMP software.

Daily monitoring of wafer manufacturing and product assembly is not the role of JMP software. This is accomplished by static and dynamic web based reports. They allow the engineers to get a quick look at their products.



There are 2 areas where daily monitoring is not enough, New Product Introduction (NPI) and Yield Enhancement (YE).

At Freescale, YE is the primary area where JMP software is utilized.

Time is Money

The winner in the semiconductor business is the company that can make "more correct decisions, faster<u>.</u>"

When a product line experiences a drop in yield, or when the yield for a product has not reached its yield potential, the YE team comes into play. They need to determine the root cause of the yield problems and they need to determine them quickly. In the semiconductor market, the value of a part is based upon the value of the technology and the value of any given technology is always dropping. Therefore, one wants to have their part yielding at a very high rate, early in the market window for the given technology. When there is a dip in the expected yield for a product ("Yield Bust") (time to detection) the determination of the root cause, (time to repair) is critical.

The 3 Parts of YE

The 3 parts required for successful YE are:

- 1. Access to the data
- 2. Data analysis
- 3. Data presentation

Access to the Data

Freescale has implemented an enterprisewide data warehouse based upon a Teradata backbone. The goal is to have all of the key manufacturing and test data from all of the steps within product fabrication fed into the warehouse. Currently, the implementation has the vast majority of the data being loaded.

For the most part, YE engineers can get all of the data they need from the data warehouse. While JMP software can access the data directly it was decided early on that a more generalized access to the data was needed. What was needed was an extraction tool that allowed an easy point and click access to extract various combinations of data that might be required and to make that data available to more than just one analysis tool. A web_based tool called GEM (Generic Extraction Module) was developed. It interfaced to the data warehouse and allowed the extraction of data directly into downstream tools, one of which is JMP software.

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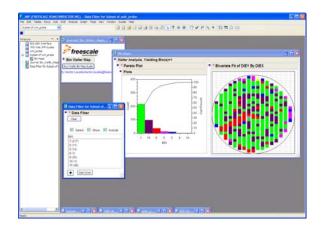
Data Analysis

JMP software was not the immediate choice of a tool for YE. JMP software is not a "Semiconductor Analysis Software Product". It is a generic data analysis software product. What the engineers need is statistical analysis, quick and easy data visualization and quick and easy specialized data visualization. Without a doubt, release 7 of JMP software met the statistical analysis need and the basic needs of the quick and easy data visualization. And, if an engineer wanted to take the time, they could approximate the required specialized visualization needs.

But the economic and industry environment does not allow the luxury of time to the engineers. Therefore, in order to make JMP software an acceptable visualization tool, several enhancements had to be made to JMP software, using JSL.

The first analysis performed by a YE engineer is a visualization called a wafer

map. Several scripts have been written to make the visualization of a wafer map a couple of clicks for the engineer.



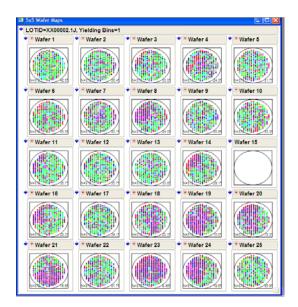
We chose to make the scripts available from a JMP software pull down menu, but stored on a centralized web page. Referred to as "Guides" the engineers simply go to the webpage and select the guide they want. The typical guide loads a JMP software journal into their JMP software session.

The journal contains a description of the guide, the instructions on how to do the analysis manually, and a button to run the already developed script.



Within Freescale, we are attempting to standardize the column names for the exported JMP software data tables. Therefore, most of the dialog boxes that are displayed for user input will have preselected choices made for the engineers. All that will remain_is for the engineer to fill in any missing information, and to click on the OK button.

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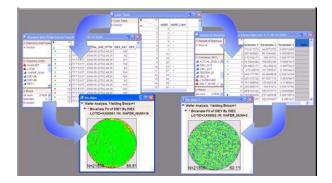
What is displayed in the above graphic is what is known in Freescale as a 5x5 Bin Wafer Map. It displays all of the wafers within a lot, and the final bin assigned to each die at the end of the wafer fabrication steps.

What is not seen is where the assigned colors for each of the bins come from. Yes, the wafer map does use the Value Colors for the bin column in the data table, and yes, the engineer can enter in the Value Colors using the Column Properties dialog box under the Column Info for the bin column. However, since the engineer will be analyzing many different lots, this process needed to be made quicker and easier.

A pair of Guides have been written that allow the engineer to save the bin color mappings in row state columns in a JMP software data table, and then to apply the stored colors onto any data table.

The first Guide takes the values from an existing data table's bin column, and generates the bin color data table.

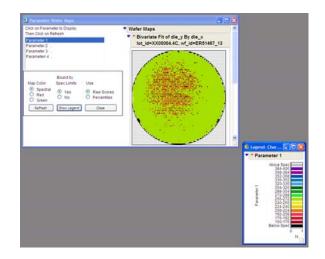
The bin color table is designed to allow the engineer to have as many bin color pairs as required to map to whatever number of different products they are working on.



The second guide takes the data from the bin color data table and applies it to the Value Colors of the bin column in the active data table.

The future plans are to enhance the GEM data extraction to directly populate the Value Colors for any bin column extracted. This remains a work in progress.

The evaluation of the spatial patterns of bins on a bin wafer map may lead to the need to look at more detailed data. One method closely related is to look at the electrical measurements for the same die on a wafer map. Since there are many different electrical measurement of interest, they want to look at the wafer maps in quick succession. Thus, this is the reason for the design of the Parametric Wafer Map Guide.

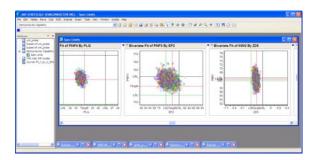


The above graphic shows a gradient pattern for a given parameter, along with a displayed legend for the gradient. One will note that the top gradient and the bottom gradient are for values that fall outside of the defined specification limits. Spec limits are very essential for data visualizations in Freescale. JMP software, while it provides a Column Property to store the limits, and does use them in the Capability analysis areas and in the Control Chart areas within JMP software, it does not surface them in all of the areas desired within Freescale. Just like the Value Colors, it does not provide a "Library" function to independently store limits that can be applied to future data tables.

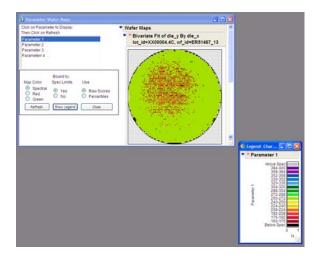
Therefore, a subsystem similar to the bin color guide has been developed for limits within Freescale.

Limits Table								
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			Limit Type	Control Limit Type	Lower Limit	Target	Upper Limit	
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		PNP1	Spec		164.389518	297.017932	429.545345	
		PNP2	Spec			455.441999		
		1/21/2	Spec		95.5938055	113.749002	130 904 138	
		PraP3	Spec			130.289793		
	6	I/P1	Spec		59.6200699	53,4101104	67.2001519	
		PH/P4	Bpec			238.736594	531.90011	
		1/P113	Spec			120.004673		
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Lower Limit	13	0.012	Spec		63.0010374	54.490468	45.1798987	
d Tarpet	14	VPII1	Spec		-80	-80	-80	
 Upper Limit 	15	1PM2	Spec		0	0	0	
	10	UPU3	Spec.		-77.085919	-60.068891	-43.053813	
	17	PMB1	Spec.		-50	-50	-50	
	18	57441	Spec		14	14	14	
	12	SPUT	Spec		-12.314665	-17.828847	-16 343009	
	20	11P115	Spec		13.7475370	13.9257051	14.1038723	
	21	EP2	Spec		73 3090808	75.2585064	79,2061119	
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	25	C4P	Spec		37 4721761	37.7355027	37.9988294	
	25	F842	Spec		94 1003544	100 241903	106 383452	
	27	PLG 2	Spec		110.400525	131.717758	143 965984	
	28	F73P5	Spec		-81 7771	-28.6145	-41.0327	
	20	10710	Spec		43.8948007	44.3007261	44.8855515	
	30	PNP6	Bpec .		0	8	0	
	31	PHIP7	Spec		-18 525215	-15.748589	-12 972113	
	22	109117	Spec		8 34545577	24.4252911	40.5351154	
	33	ProPil	Spec		-47.947013	-40.507858	-33 068703	

Also, the Fit Y by X platform has been augmented to display spec limits and targets on the graphical output.

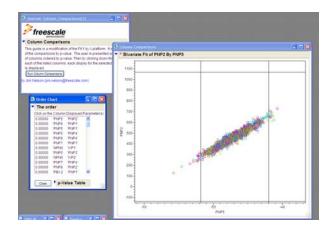


Returning to the Parametric Wafer Map Guide, another feature needs to be pointed out.



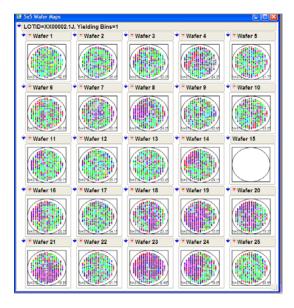
The displayed wafer map can switch between different parameters very quickly. This methodology is a big requirement for Freescale engineers. They want to look for patterns and for things that fall outside of their "engineering experience knowledge basis" of what is normal.

While multivariate methodologies do exist that may provide similar results, the Freescale engineering community tends to be more comfortable with the more tangible results from univariate and bivariate analysis. To provide this same methodology in the bivariate space, The Fit Y by X platform has been modified to allow the engineer to select any number of X and Y columns and then for the p-Values for the various combinations and permutations are calculated. The p-Values are then sorted and the columns displayed in a sorted list. The engineers can then quickly move from one display to another by simply clicking on the parameter combination they wish to display.



Data Presentation

JMP software provides a strong cut and paste and "Save As" interface between the various outputs and the "Freescale Management Presentation System". FMPS, more commonly referred to as MS Word, PowerPoint and Excel are where the majority of JMP software results end up. While the platform output from JMP software very nicely provides easy selection of what is to be copied and pasted, we have had to become experts at providing Outline Boxes in the developed scripts that make the selections quick and easy for the engineer. An attempt is made to put Outline Boxes in all of the logical places of output.



As can be seen in the above 5x5 wafer map, there are 25 bivariate platform outputs. While those outputs contain the results desired by the engineers, by adding an Outline Box to the scripts output, the complete 5x5 output can be selected with 1 click and then copies and pasted to FMPS.

Rolling it all Out

The semiconductor industry is a high pressure industry. When you couple that with today's economic environment, getting an engineer to change what they are knowledgeable and comfortable in using to get their jobs done is very difficult and resource intensive. During the initial rollout of the data warehouse in Freescale, the typical rounds of training were completed on the new products and methods that were now available to the engineers. Subsequent metrics on the usage of the new tools a data fell far below the projected levels. Investigation of the issues clearly pointed to the fact that Freescale engineers do not have the time to do self investigation and learning of new tools and methodologies. Therefore, we have had to move to a far more resource intensive, proactive approach.

We have had to move to working directly with 1-5 individuals that all have common analysis needs. We need to show them the precise advantage they will gain in using the new warehouse and JMP software tools.



Everett Rogers: Adoption Innovation Model

We have moved past the area of Early Adopters and into the Early Majority. The requirement to get them to change is to show them the errors of their current ways. With the engineering community at Freescale and the pressures they are under, this is a daunting task. The commitment of valuable resources to the training of end users as well as "Training the Trainers" is what Freescale committed itself to do to get the product rolled out.

Conclusions

While JMP software releases 6, 7 and now 8 have really moved JMP software into the world of Data Visualization, many of the Specialized Visualizations required for the semiconductor industry had to be developed in-house to make JMP software a standard YE tool within Freescale. The fact that JSL is there and is as powerful as it is, has allowed those visualizations to be added to JMP software and for it in turn to become one of the key YE tools within Freescale Semiconductor.