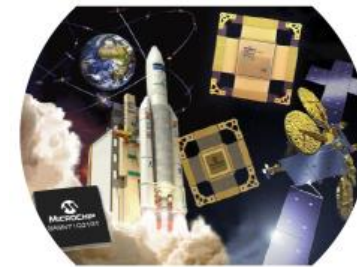


# Development of Predictive Single Event Latchup Model



**Aerospace &  
Defense Group**

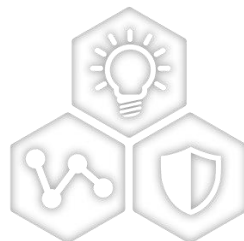


---

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



**Aerospace &  
Defense Group**



SMART | CONNECTED | SECURE

**Laurence Montagner**

March 2023

# SELEST

- **Development of internal SEL prediction tool funded by the CNES, French space agency**



- **2 posters presented at RADECS (2019 and 2021)**

New Approach of Single Event Latchup Modeling Based on TCAD Simulations and Design of Experiment Analysis

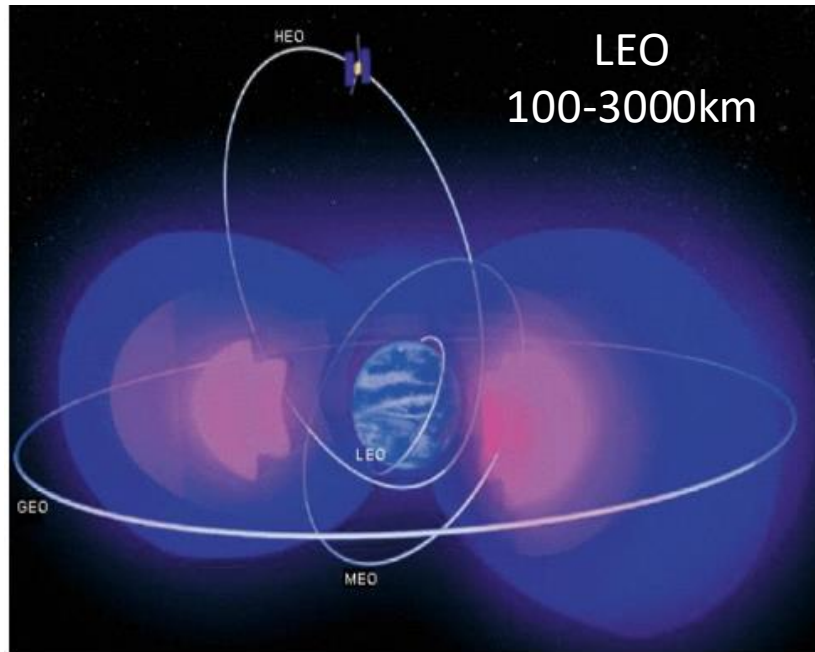
*D. Truyen, L.Montagner*

A Neural Network Approach for Single-Event Latchup Prediction Based on TCAD Simulations in CMOS Technology

*D. Truyen, E Leduc, L.Montagner, M.Briet, A. Collange*

# Context

- To address the new space market “low cost”, COTS (circuits on the shelves) are evaluated and “hardened” to radiation to meet space agency specifications.  
→ Need to analyze of a lot of products to estimate quickly their radiation behaviour and their ability to be hardened before any expensive experimental test.



**GEO** : Geosynchronous Earth Orbit  
**MEO** : Medium Earth Orbit

**LEO** : Elliptica Low Earth Orbit  
**HEO** : Highly l Orbit



# Context

## Radiations impact on Electronic Circuits

### 1- The sun



### 2- Cosmic Rays

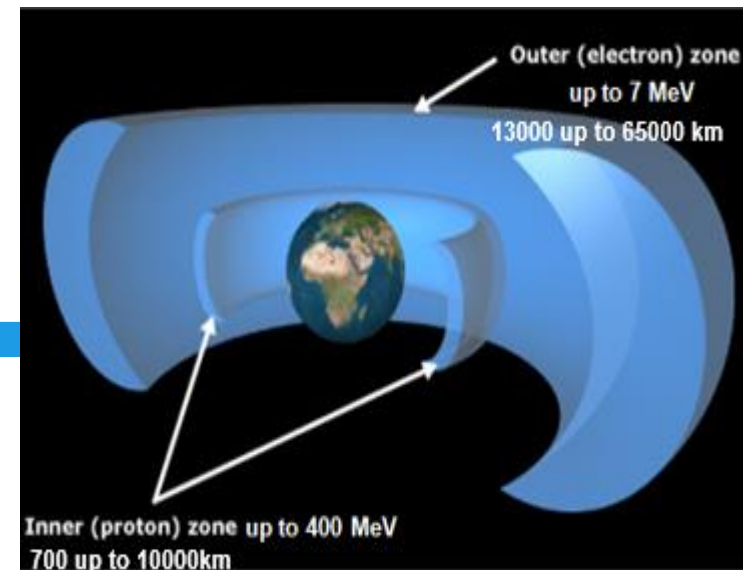


Radiation effects

**SEE / TID**



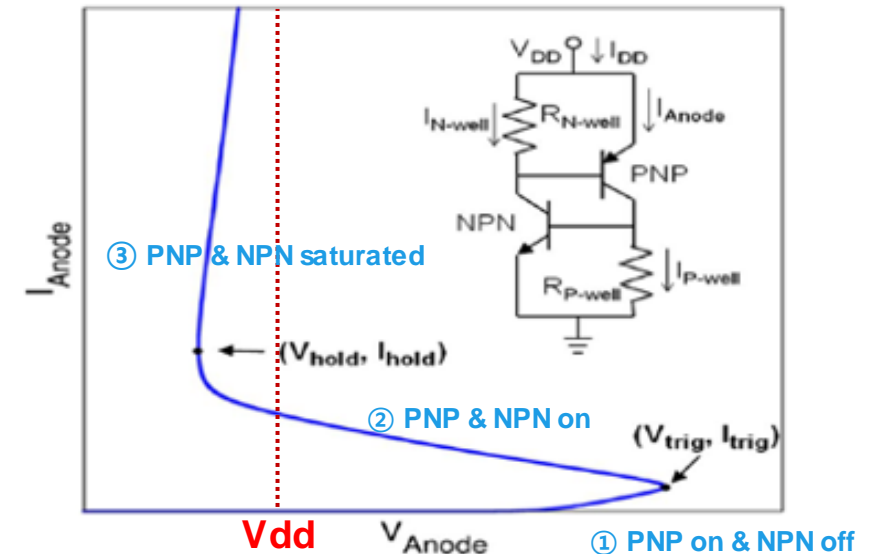
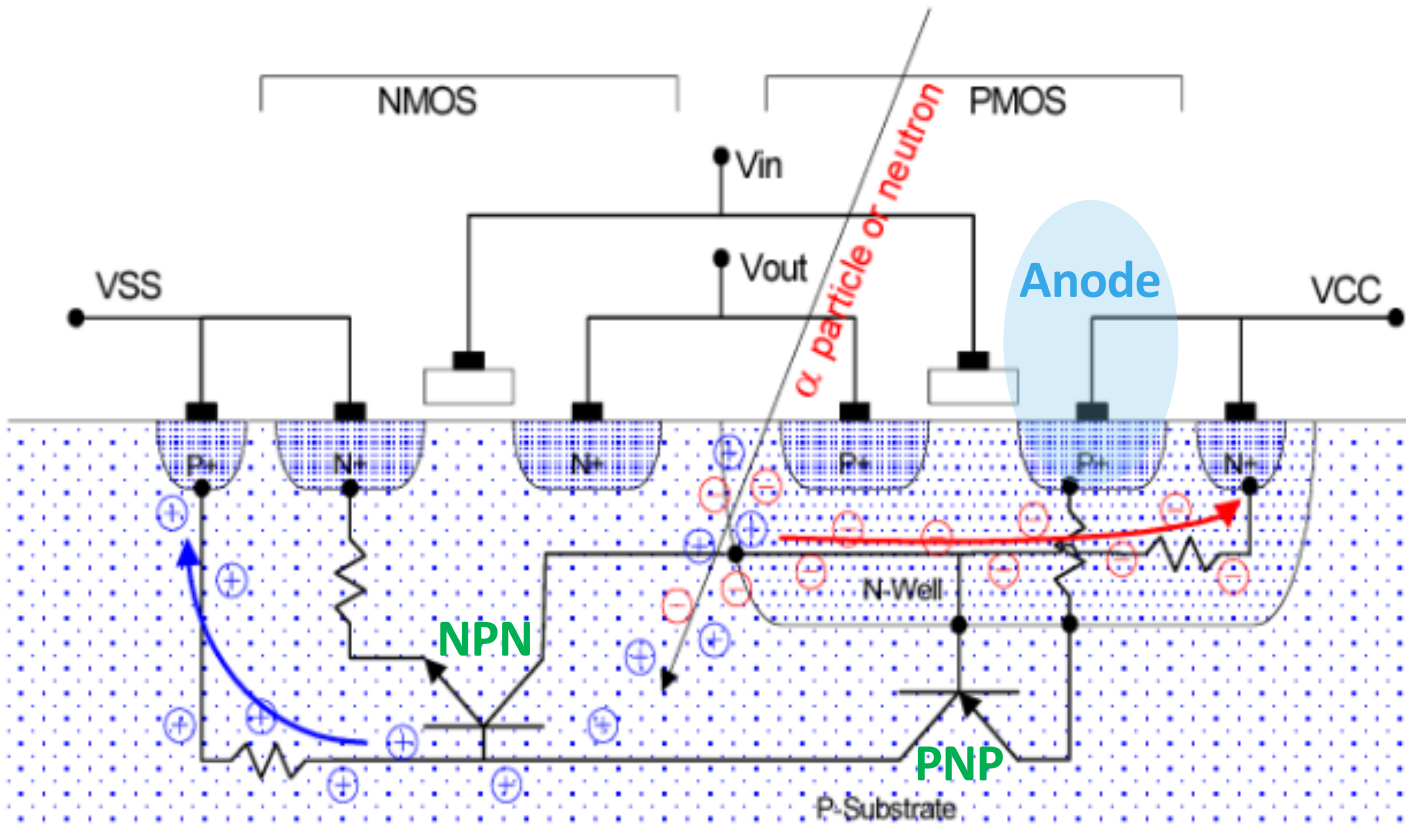
### 3- Van Allen Belts



# Focus on Single Event Latchup (SEL)

## Mechanism

- SEL is a critical effect with catastrophic impact on space craft systems
- SEL is a triggering of the parasitic thyristor (2 parasitic bipolars: NPN & PNP)



If an energetic particle produces:

- $I_{Anode} > I_{trig}$
  - $\beta_n \cdot \beta_p > 1$
  - $V_{DD} > V_{hold}$
- SEL will occur**

# Single Event Effects – Charged Particles

## Linear Energy Transfer - LET

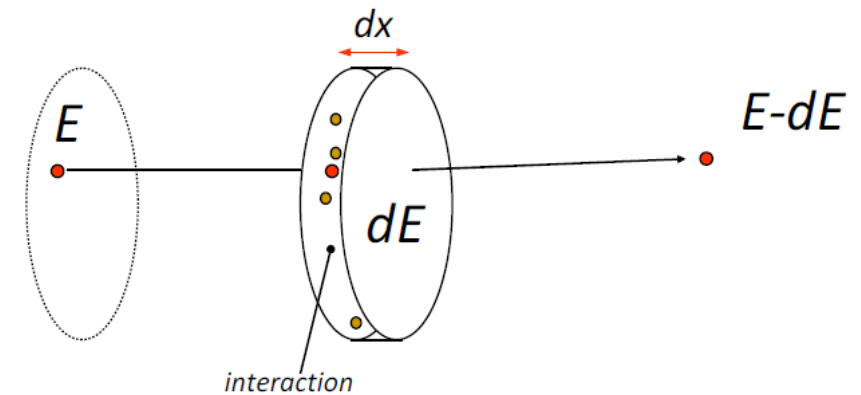
- **Direct ionization (ions): Linear Energy Transfer electronic (LET)**

Heavy-ions are described by amount of energy lost in the matter per unit track length in the considered material

**LET:**

- $dE/dx = \text{MeV/cm}$
- Material density =  $\text{mg/cm}^3$

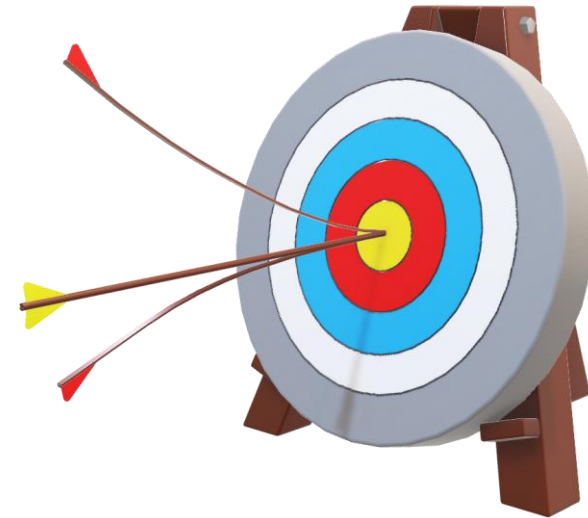
$$LET = \frac{dE}{dx} \times \frac{1}{\rho} \Rightarrow \frac{\text{MeV}}{\text{cm}} \times \frac{1}{\frac{\text{mg}}{\text{cm}^3}} \Rightarrow \text{MeV} \cdot \text{cm}^2 / \text{mg}$$



- The parasitic currents increase with the LET
  - $100 \text{ MeV} \cdot \text{cm}^2 / \text{mg} = \sim 1 \text{ pC} / \mu\text{m}$  in the Silicon
- ESA Criteria: immune to latchup  $>60 \text{ MeV} \cdot \text{cm}^2 / \text{mg}$

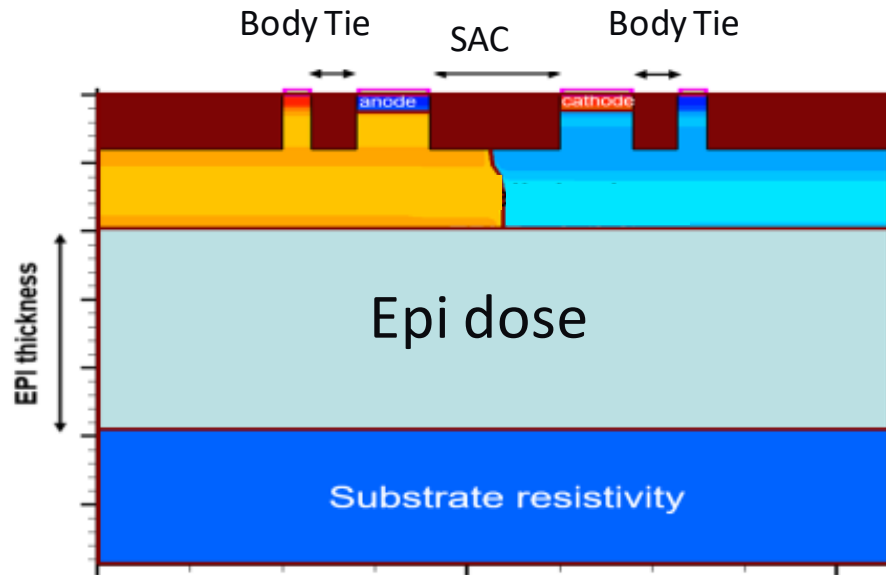
# Objective

- ❑ Implementation of an analytical prediction model based on calibrated simulation
  
- ❑ Prediction of SEL sensitivity :
  - Vhold
  - LETth



# Input and Output definition

- TCAD Sentaurus view of inverter



Input	Output
SAC	$V_{hold}$
Body Tie	LET <sub>th</sub>
Epi Thickness	
Epi dose	

LET<sub>th</sub>,  $V_{hold}$

$V_{hold} > V_{cc} \rightarrow$  No SEL, LET<sub>th</sub> > 60 MeV.cm<sup>2</sup>/mg

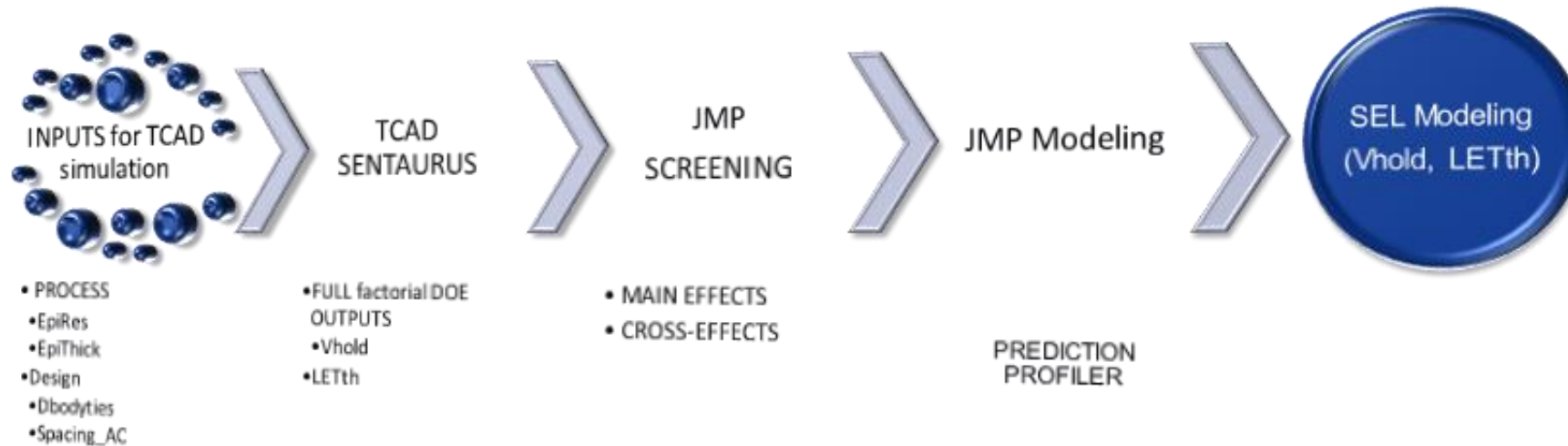
$V_{hold} < V_{cc} \rightarrow$  SEL possible, LET<sub>th</sub> ?  $\rightarrow$  LET<sub>th</sub> Model



# SEL Modeling Flow

## Model for SEL prediction:

- LETth and Vhold Versus Input parameters

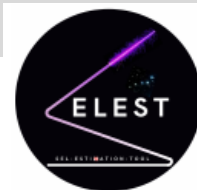


# Model validation with experimental results

A Neural Network Approach for Single-Event Latchup Prediction Based on TCAD Simulations in CMOS Technology

*D. Truyen, E Leduc, L.Montagner, M.Briet, A. Collange*

Modification of DOE by adding inputs per technology node for better accuracy  
Use of neural network models



Version 2

SUMMARY OF HEAVY ION SEL, AND COMPARISON WITH PREDICTIVE MODEL

Products	Tech. node (μm)	SEL LET <sub>th</sub> (MeV.cm <sup>2</sup> /mg)	
		Pred. Model <i>SELEST</i>	Exp.
<i>16-Bit Microcontroller Dual Core</i>	0.09	12.06	< 3.3
<i>16-Bit SPI I/O Expander with Open-Drain Output</i>	0.6	0.34	4.2
<i>16-Bit digital Signal Controller for digital power Applications</i>	0.18	2.64	< 3.6
<i>64-Mbit Serial Quad I/O (SQI) Flash Memory</i>	0.07	62.3	> 78
<i>Ethernet physical layer transceiver</i>	0.065	65.6	64
<i>8-Bit Microcontroller</i>	0.18	33.5	39

**Thanks for your attention**